Patent claims

1. A method for picture-in-picture insertion,
in which a sequence of decimated inset pictures is written to a memory device (2) and is read out for insertion into a sequence of main pictures,
characterized
in that the inset pictures are written to the memory device (2) in a circulating manner as fields under continuously incremented write addresses, the inset pictures being written to corresponding memory segments beginning at corresponding writing start addresses,
in that the writing start address of each written-in field is stored,
in that, each time the write address is incremented, by comparison of the respective instantaneous write address with a previously stored writing start address, an overtake signal is formed which indicates whether the respective writing start address is reached again and the memory segment corresponding to the respective writing start address is overwritten,
in that, by evaluation of the overtake signal, the memory segment corresponding to the last writing start address stored or the penultimate writing start address stored is selected for read-out, and
in that the selected memory segment is read out for insertion into the respective main picture with continuously incremented read addresses.

2. The method as claimed in claim 1,
characterized in that the write and read addresses are continuously incremented from a first memory address up to a last memory address and are in each case reset to the first memory address again after the last memory address has been reached.

3. The method as claimed in claim 1 or 2,
characterized in that, in order to insert an inset picture into a main picture, in a segment buffer (7) for two inset pictures, the picture position and size are in each case stored in the form of a number of lines and also pixels per line.

4. The method as claimed in one of the preceding claims,
characterized in that raster correction is effected by comparison between the raster position of a picture to be displayed and the raster position of a stored picture and also by skipping or repeating a line.

5. The method as claimed in one of the preceding claims,
characterized
in that, each time the write address is incremented, the instantaneous write address is compared with the penultimate writing start address stored and, in the event of correspondence, the last writing start address stored is used as reading start address for reading the corresponding memory segment, whereas otherwise the penultimate writing start address is used as reading start address for reading the corresponding memory segment.

6. A circuit arrangement for inserting a sequence of decimated inset pictures into a sequence of main pictures,
having a write controller (4) for writing the inset pictures as fields under continuously incremented write addresses to corresponding memory segments of a memory device (2) beginning at corresponding writing start addresses,

having a segment buffer (7) for storing the writing start address of each field written to the memory device (2), in which case an overtake signal can be generated by the write controller (4) each time the write address is incremented, by comparing the respective instantaneous write address with a previously stored writing start address, which overtake signal indicates whether the respective writing start address is reached again and the memory segment of the memory device (2) which corresponds to the respective writing start address is overwritten,

having a display controller (6) to which the overtake signal is fed, in which case the display controller (6) can select, by evaluating the overtake signal, the memory segment corresponding to the last writing start address stored or the penultimate writing start address stored, for read-out by a read controller (5) - connected to the segment buffer (7) - with the aid of continuously incremented read addresses and for insertion into the respective main picture.

7. The circuit arrangement as claimed in claim 6, characterized in that the write controller (4) and the read controller (5) each have an address counter (12) for incrementing the write addresses and read addresses, respectively.

8. The circuit arrangement as claimed in claim 6 or 7,

characterized in that, by means of the display controller (6), an insertion position of an inset picture is calculated and a corresponding insertion signal can be fed to an insertion apparatus (3).

9. The circuit arrangement as claimed in one of claims 6 to 8,

characterized in that, by means of the display controller (6), raster correction can be carried out by comparison between the raster position of a picture to be displayed and the raster position of a stored picture and also by skipping or repeating a line.

10. The circuit arrangement as claimed in one of claims 6-9,
characterized
in that provision is made of a comparator (14) for comparing the instantaneous write address provided by an address counter (12) with the penultimate writing start address stored, the output of the comparator (14) being connected to a flip-slop (15) for driving a multiplexer (13), and
in that the penultimate writing start address stored is present at a first input of the multiplexer (13) and the last writing start address stored is present at a second input of the multiplexer (13), with the result that, in the event of correspondence between the instantaneous write address of the address counter (12) and the penultimate writing start address stored, the multiplexer (13) outputs the last writing start address stored as reading start address, whereas otherwise the multiplexer (13) outputs the penultimate writing start address stored as reading start address.

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